

ABSTRACT OF THE DISCLOSURE

A semiconductor device has an isolation area having a shallow trench isolation (STI) structure for isolating device areas for transistor elements. The isolation area for a bipolar transistor has a first annular trench encircling a n-type collector well, a second annular trench encircling the first annular trench and an annular p-type diffused region disposed between the first annular trench and the second annular trench while in contact with the annular trenches. The plurality of isolation trenches in a single isolation area prevents a dishing portion of the substrate after a CMP process without causing a short-circuit failure.

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